ANALOG DEVICES

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

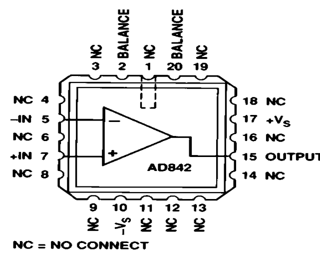
AC PERFORMANCE
Gain Bandwidth Product: 80 MHz (Gain = 2)
Fast Settling: 100 ns to 0.01% for a 10 V Step
Slew Rate: 375 V/µs
Stable at Gains of 2 or Greater
Full Power Bandwidth: 6.0 MHz for 20 V p-p

DC PERFORMANCE
Input Offset Voltage: 1 mV max
Input Offset Drift: 14 µV/°C
Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
Open-Loop Gain: 90 V/mV into a 500 Ω Load
Output Current: 100 mA min
Quiescent Supply Current: 14 mA max

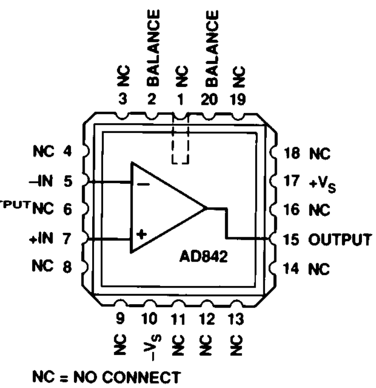
APPLICATIONS
Line Drivers
DAC and ADC Buffers
Video and Pulse Amplifiers
Available in Plastic DIP, Hermetic Metal Can, Hermetic Cerdip, SOIC and LCC Packages and in Chip Form
MIL-STD-883B Parts Available
Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAMS

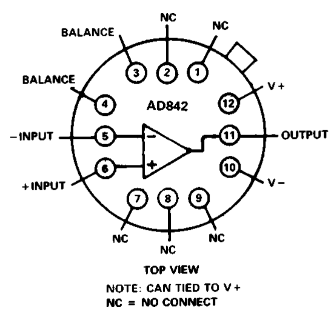
Plastic DIP (N) Package and Cerdip (Q) Package



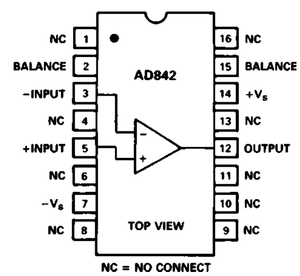
LCC (E) Package



TO-8 (H) Package



SOIC (R-16) Package



PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/µs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

REV. D

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Tel: 617/329-4700 Fax: 617/326-8703

AD842–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J/JR[1] Min	Typ	Max	AD842K Min	Typ	Max	AD842S[2] Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[3]			0.5	**1.5**		0.3	**1.0**		0.5	**1.5**	mV
	T_{MIN}–T_{MAX}			2.5/3			**1.5**			3.5	mV
Offset Drift			14			14			14		μV/°C
INPUT BIAS CURRENT			4.2	**8**		3.5	**5**		4.2	**8**	μA
	T_{MIN}–T_{MAX}			10			**6**			**12**	μA
Input Offset Current			0.1	**0.4**		0.05	**0.2**		0.1	**0.4**	μA
	T_{MIN}–T_{MAX}			0.5			**0.3**			**0.6**	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	115		**90**	115		**86**	115		dB
	T_{MIN}–T_{MAX}	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		μV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 500 Ω	**40/30**	90		**50**	90		**40**	90		V/mV
	T_{MIN}–T_{MAX}	20/15			**25**			**20**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**100**			**100**			**100**			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[4]	V_O = 20 V p-p										
	R_{LOAD} ≥ 500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[5]	A_{VCL} = –2		10			10			10		ns
Overshoot[5]	A_{VCL} = –2		20			20			20		%
Slew Rate[5]	A_{VCL} = –2	300	375		300	375		300	375		V/μs
Settling Time[5]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			13/14	**14/16**		13	**14**		13	**14**	mA
	T_{MIN}–T_{MAX}			16/19.5			**16**			**19**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	105		**86**	100		dB
	T_{MIN}–T_{MAX}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[6]		0		+75	0		+75	–55		+125	°C
PACKAGE OPTIONS											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ, AD842SQ/883B		
SOIC (R-16)			AD842JR-16								
Tape and Reel			AD842JR-16-REEL								
			AD842JR-16-REEL7								
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC (E-20A)									AD842SE/883B		
Chips			AD842JCHIPS						AD842SCHIPS		

NOTES

[1] AD842JR specifications differ from those of the AD842JN, JQ and JH due to the thermal characteristics of the SOIC package.

[2] Standard Military Drawing available 5962-8964201xx
2A – (SE/883B); XA – (SH/883B); CA – (SQ/883B).

[3] Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[4] Full power bandwidth = slew rate/2 π V_{PEAK}.

[5] Refer to Figures 22 and 23.

[6] "S" grade T_{MIN}–T_{MAX} specifications are tested with automatic test equipment at T_A = –55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
Plastic (N)	1.3 W
Cerdip (Q)	1.1 W
TO-8 (H)	1.3 W
SOIC (R)	1.3 W
LCC (E)	1.0 W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range	
Q, H, E	–65°C to +150°C
N	–65°C to +125°C
Junction Temperature	+175°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Maximum internal power dissipation is specified so that T_J does not exceed +150°C at an ambient temperature of +25°C.

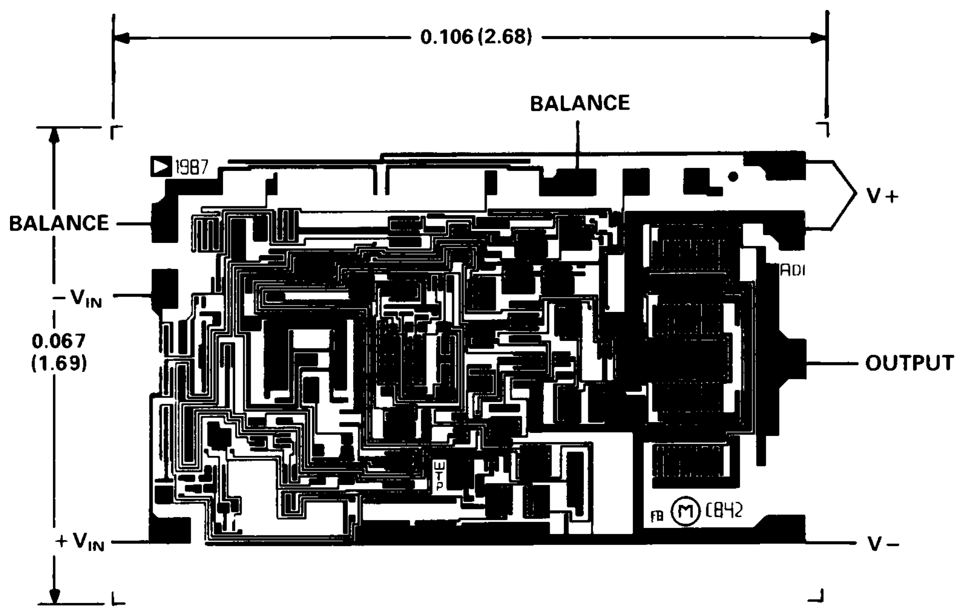
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}
Plastic Package	30°C/W	100°C/W	
Cerdip Package	30°C/W	110°C/W	38°C/W
TO-8 Package	30°C/W	100°C/W	27°C/W
16-Pin SOIC Package	30°C/W	100°C/W	
20-Pin LCC Package	35°C/W	150°C/W	

Recommended Heat Sink: Aavid Engineering© #602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



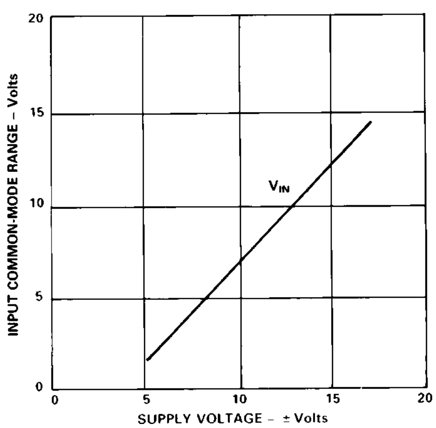


Figure 1. Input Common-Mode Range vs. Supply Voltage

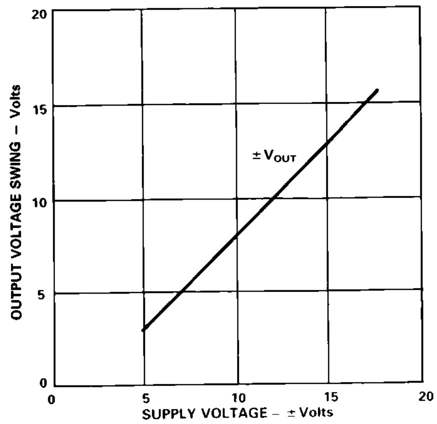


Figure 2. Output Voltage Swing vs. Supply Voltage

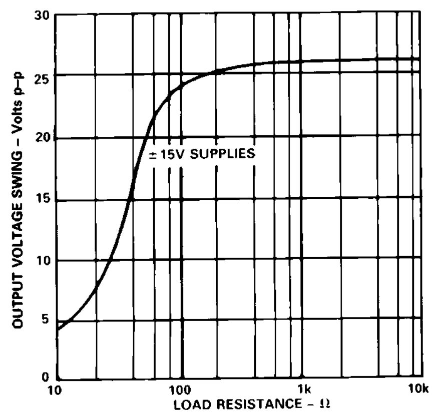


Figure 3. Output Voltage Swing vs. Load Resistance

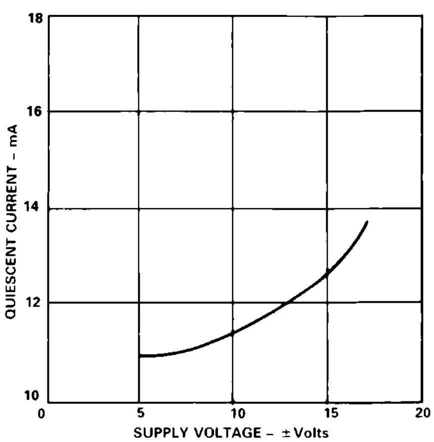


Figure 4. Quiescent Current vs. Supply Voltage

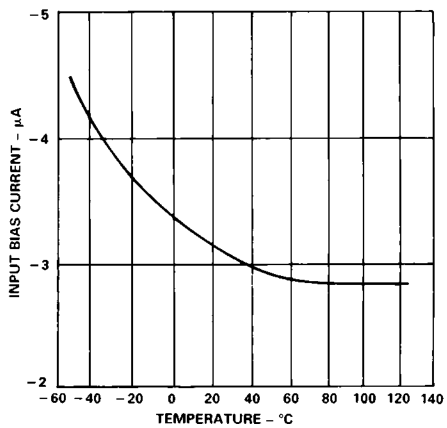


Figure 5. Input Bias Current vs. Temperature

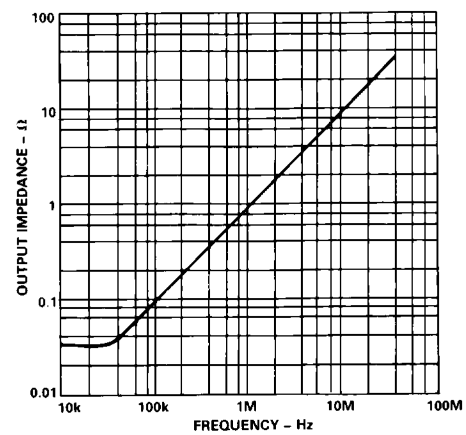


Figure 6. Output Impedance vs. Frequency

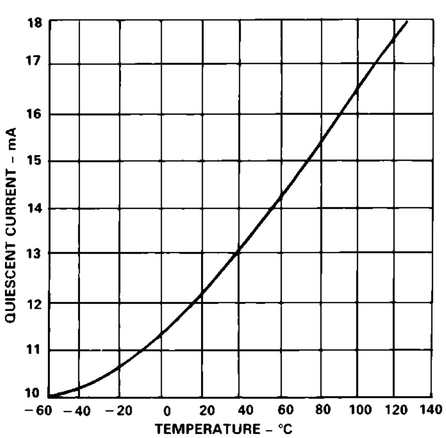


Figure 7. Quiescent Current vs. Temperature

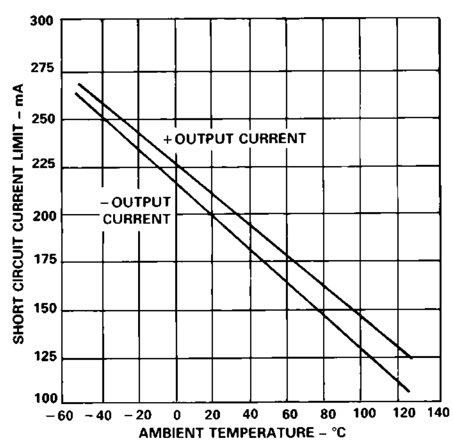


Figure 8. Short-Circuit Current Limit vs. Temperature

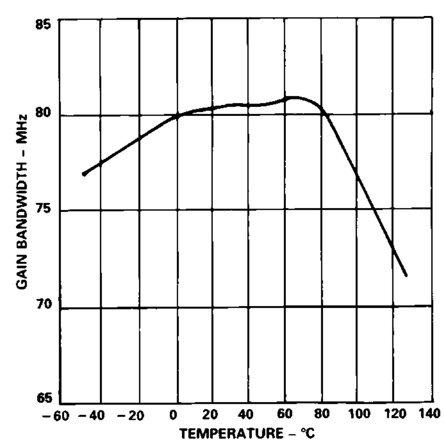


Figure 9. Gain Bandwidth Product vs. Temperature

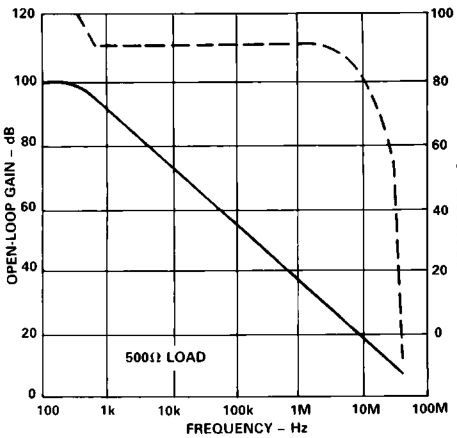


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

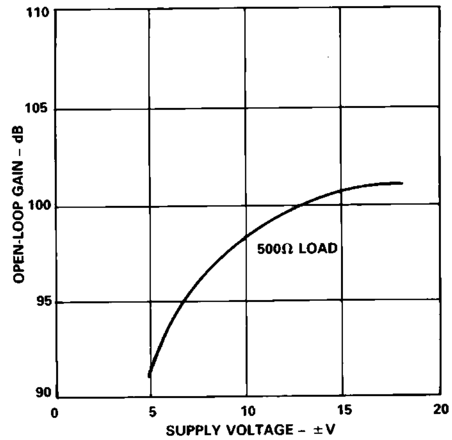


Figure 11. Open-Loop Gain vs. Supply Voltage

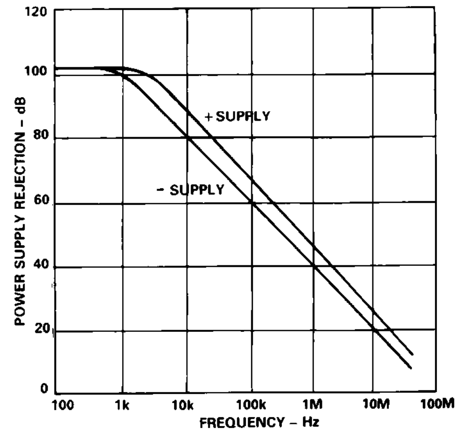


Figure 12. Power Supply Rejection vs. Frequency

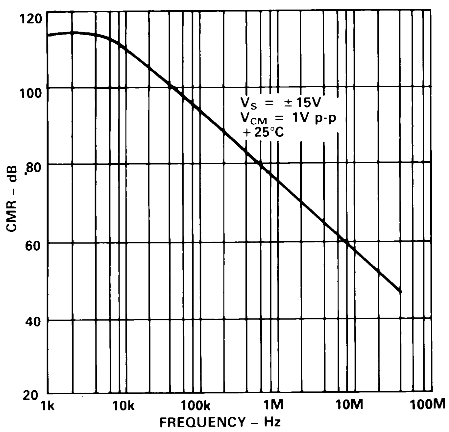


Figure 13. Common-Mode Rejection vs. Frequency

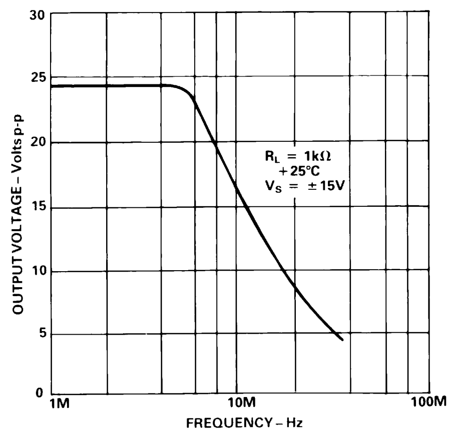


Figure 14. Large Signal Frequency Response

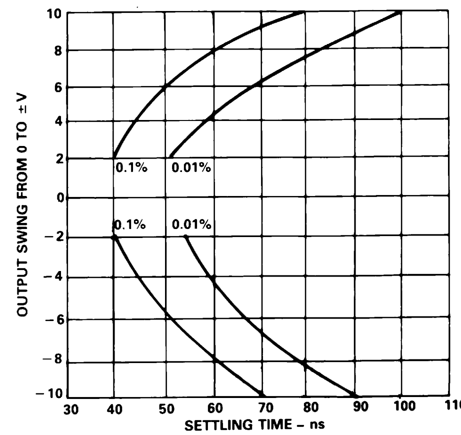


Figure 15. Output Swing and Error vs. Settling Time

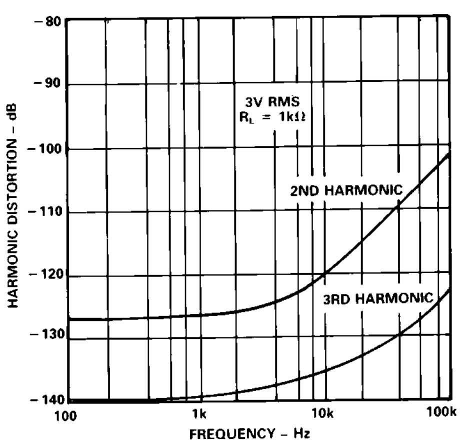


Figure 16. Harmonic Distortion vs. Frequency

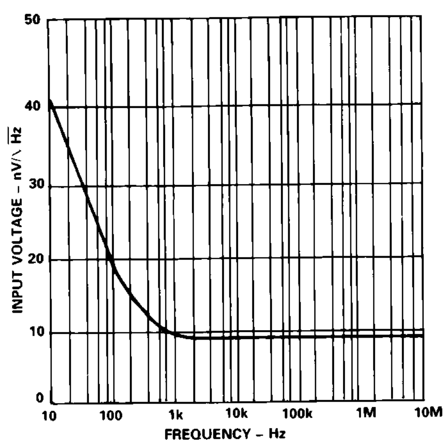


Figure 17. Input Voltage vs. Frequency

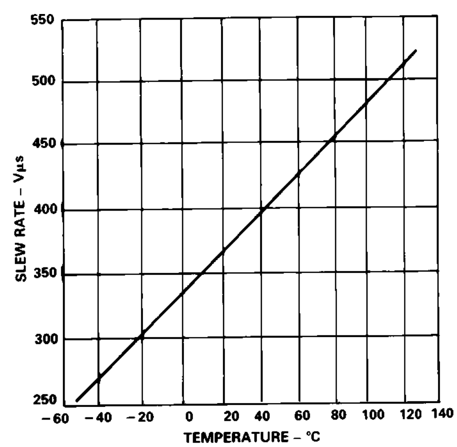


Figure 18. Slew Rate vs. Temperature

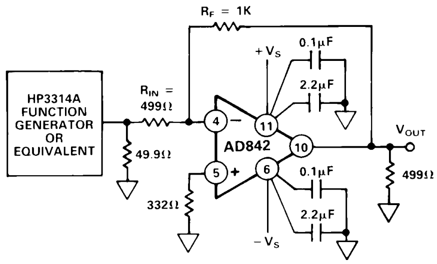


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

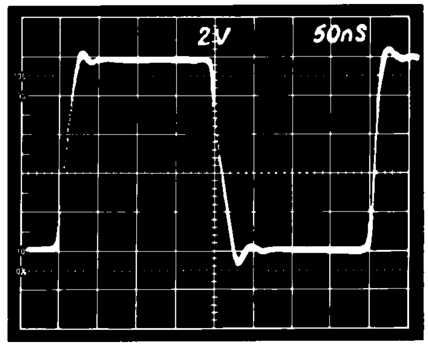


Figure 19b. Inverter Large Signal Pulse Response

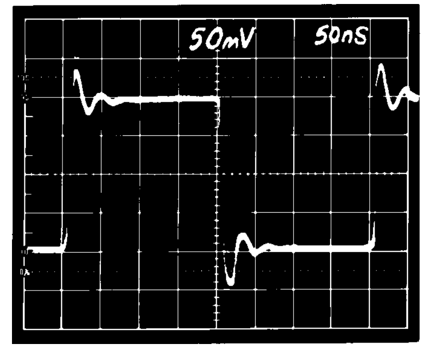


Figure 19c. Inverter Small Signal Pulse Response

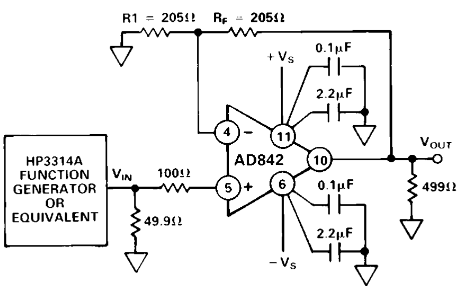


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

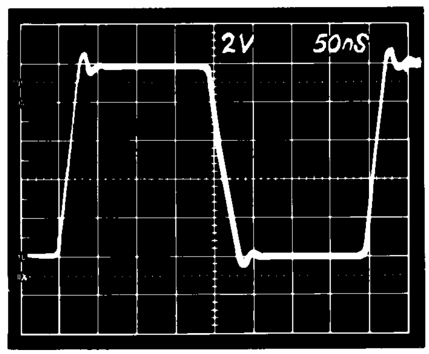


Figure 20b. Noninverting Large Signal Pulse Response

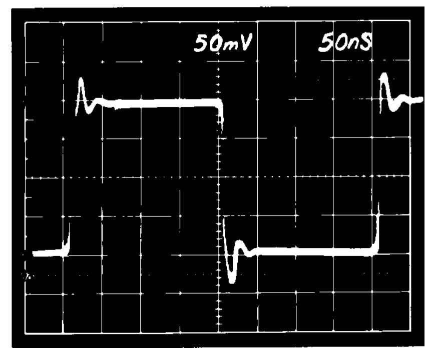


Figure 20c. Noninverting Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD842 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD842 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD842 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

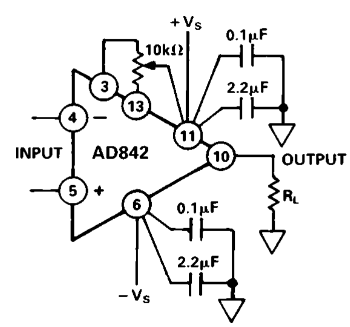


Figure 21. Offset Nulling (DIP Pinout)

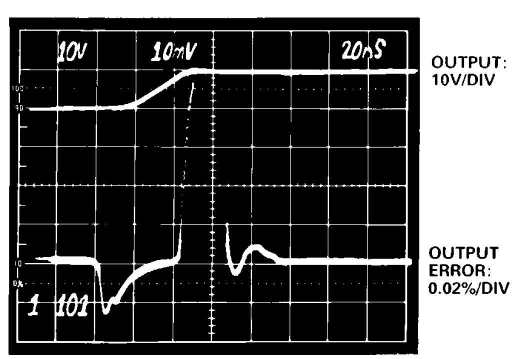


Figure 22. AD842 0.01% Settling Time

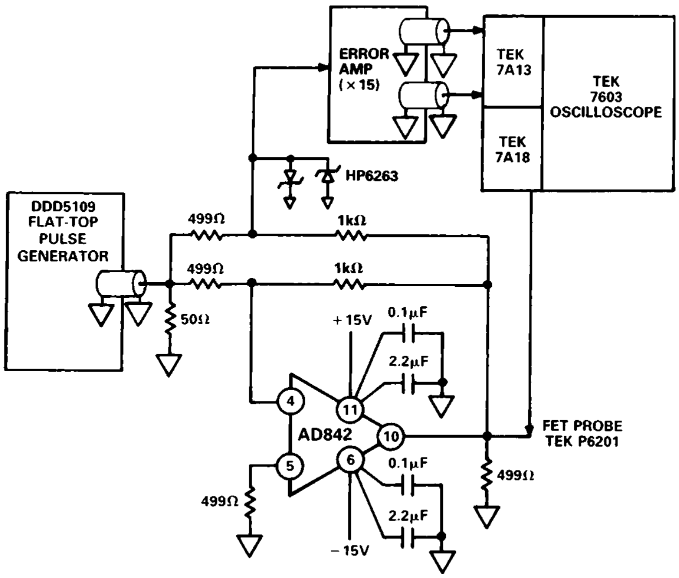


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD842's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high-speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 300 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 15, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD842 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

GROUNDING AND BYPASSING

In designing practical circuits with the AD842, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

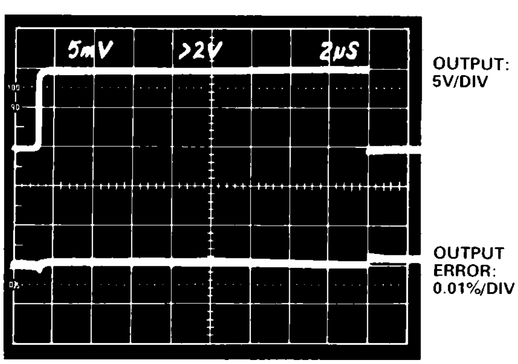


Figure 24. AD842 Settling Demonstrating No Settling Tails

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor connected in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD842 is sensitive to capacitive loading. The AD842 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF.

USING A HEAT SINK

The AD842 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 10 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD842 is optimized for high speed line driver applications. Figure 25 shows the AD842 driving a doubly terminated cable in a gain-of-2 follower configuration. The AD842 maintains a typical slew rate of 375 V/μs, which means it can drive a ±10 V, 6.0 MHz signal or a ±3 V, 19.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD842 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal. With this circuit, the voltage on the line equals V_{IN} because one half of V_{OUT} is dropped across R_{BT}.

The AD842 has ±100 mA minimum output current and, therefore, can drive ±5 V into a 50 Ω cable.

The feedback resistors, R_1 and R_2, must be chosen carefully. Large value resistors are desirable in order to limit the amount of current drawn from the amplifier output. But large resistors can cause amplifier instability because the parallel resistance $R_1 \| R_2$ combines with the input capacitance (typically 2–5 pF) to create an additional pole. Also, the voltage noise of the AD842

is equivalent to a 5 kΩ resistor, so large resistors can significantly increase the system noise. Resistor values of 1 kΩ or 2 kΩ are recommended.

If termination is not used, cables appear as capacitive loads and can be decoupled from the AD842 by a resistor in series with the output.

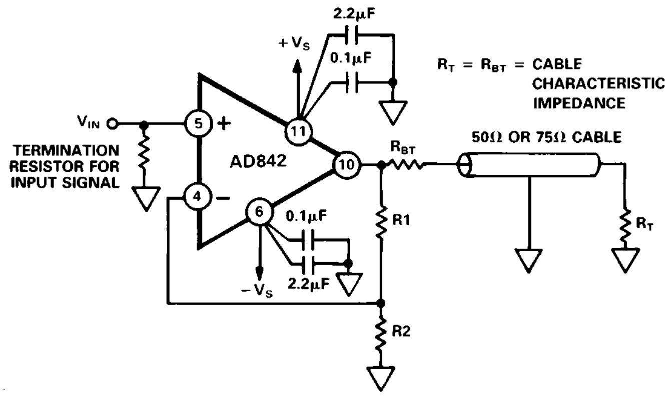


Figure 25. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD842. Typical recovery time is 80 ns from negative overdrive and 400 ns from positive overdrive.

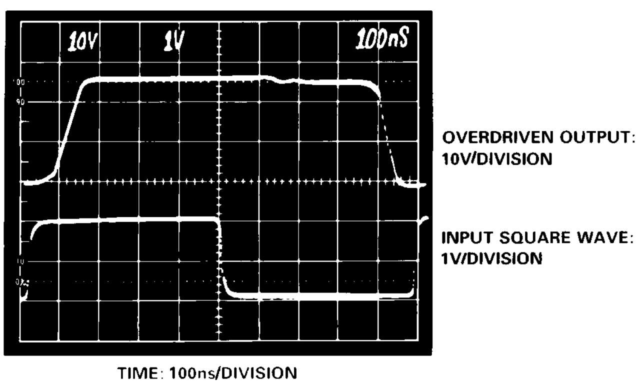


Figure 26. Overdrive Recovery

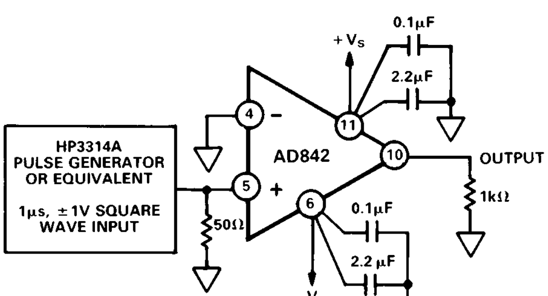
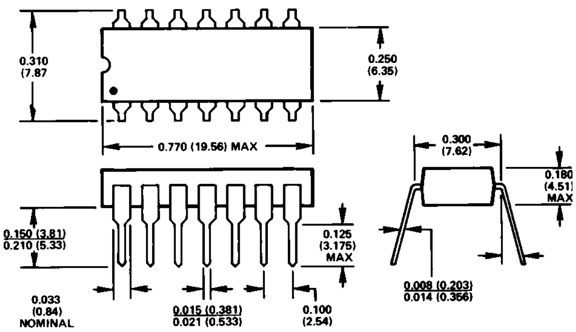


Figure 27. Overdrive Recovery Test Circuit

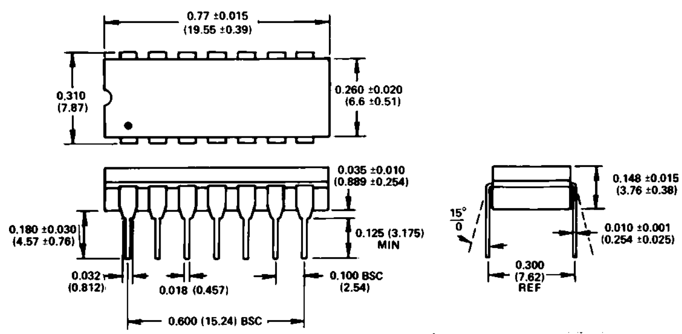
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

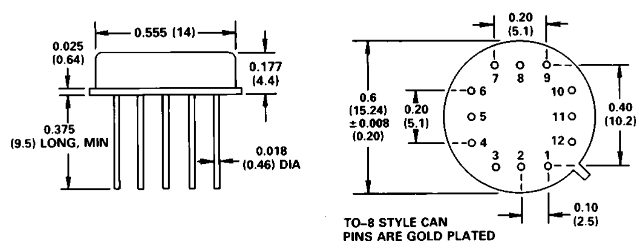
14-Pin Plastic (N) Package



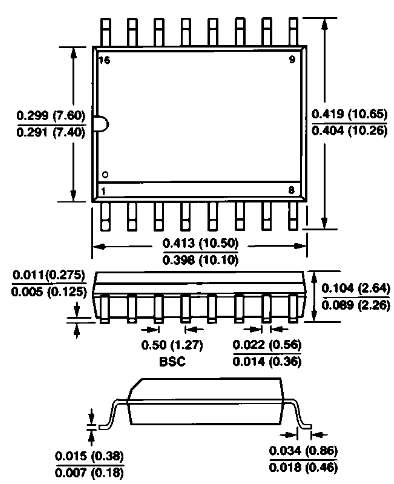
14-Pin Cerdip (Q) Package



12-Lead Metal Can Package (TO-8 Style)



16-Lead SOIC (R-16) Package



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